# Testing of Flow-Based Microfluidic Biochips: Fault Modeling, Test Generation, and Experimental Demonstration

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***Abstract*—Recent advances in flow-based microfluidics have led to the emergence of biochemistry-on-a-chip as a new paradigm in clinical diagnostics and biomolecular recognition. However, a potential roadblock in the deployment of microfluidic biochips is the lack of test techniques to screen defective devices before they are used for biochemical analysis. Defective chips lead to repetition of experiments, which is undesirable due to high reagent cost and limited availability of samples. Prior work on fault detection in biochips has been limited to digital ("droplet") microfluidics and other electrode-based technology platforms. The paper proposes the first approach for automated testing of flow-based microfluidic biochips that are designed using membrane-based valves for flow control. The proposed test technique is based on a behavioral abstraction of physical defects in microchannels and valves. The flow paths and flow control in the microfluidic device are modeled as a logic circuit composed of Boolean gates, which allows test generation to be carried out using standard automatic test pattern generation tools. The tests derived using the logic circuit model are then mapped to fluidic operations involving pumps and pressure sensors in the biochip. Feedback from pressure sensors can be compared to expected responses based on the logic circuit model, whereby the types and positions of defects are identified. We show how a fabricated biochip can be tested using the proposed method, and demonstrate experimental results for two additional fabricated chips.**

***Index Terms*—Automatic test pattern generation (ATPG), defects, fault modeling, lab-on-chip, microfluidics, testing.**

## I. Introduction

FLOW-BASED microfluidic biochips constitute an exciting emerging technology that enables the integration of fluid-handling operations [1]. Continuous liquid flow with picoliter volumes in a flow-based microfluidic biochip can be achieved in etched microchannels in the "flow layer." Through thousands of integrated microvalves in the "control layer," different fluid-handling operations, such as mixing, dilution, and transportation, can be easily implemented [2], [3].

Recent advances in fabrication techniques, including the application of polydimethylsiloxane (PDMS) and dense integration of active microvalves, have enabled the development of flow-based microfluidic biochips. These devices allow a transition from a simple topology with only a few channels to large-scale networks of channels for realistic applications [4]. Increasing integration levels provide biochips with tremendous potential; hundreds of different bioassays, i.e., protocols for biochemistry, can be processed independently, simultaneously, and automatically on a coin-sized microfluidic platform [5]. These advances therefore allow massively-parallel biochemical processing and immediate point-of-care disease diagnosis [6]. In 2011, Fluidigm, a biotech company that focuses on flow-based microfluidic biochips, launched its initial public offering at NASDAQ, which is a significant milestone in the maturation of the microfluidic industry.

Despite the above developments, the adoption of flow-based biochips is hampered by defects that are especially common for PDMS chips [7]. In addition, owing to the inherent randomness of component reactions in biochemistry, predictive modeling and accurate control are difficult [8], [9]. All these factors make biochips especially vulnerable to defects and erroneous microfluidic operations, which are unacceptable for applications such as real-time DNA sequencing [10] and antigen detection [11] that require high precision. When an unexpected error occurs, the entire experiment has to be repeated on a new chip [12]. Repetition of experiments is costly, since samples are hard to obtain and reagents are expensive. Such repetition also increases the time-to-result for clinical diagnosis.

To overcome these barriers to practical adoption and deployment, a quality-checking method is needed to target key fluidic operations before chip use [13]. Defective chips need to be identified and subsequently discarded. Furthermore, for the adoption of PDMS microfluidic technology, quality-control measurements are required. The service providers must have robust post-fabrication testing methods to ensure the quality of their product. Only then can researchers trust data generated using these devices. Recent advances in testing of digital microfluidic biochips [14]–[16] cannot be used here because of the many differences in the underlying

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technologies. Flow-based biochips manipulate continuous flow in microchannels using pumps and valves, while digital microfluidic biochips control discrete droplets on an electrode array using the principle of electrowetting-on-dielectric [17]. The test stimuli, test control, and observation methods are inherently different for these types of biochips. The fluid-control mechanism and complex microchannel network structures in flow-based devices make testing difficult.

To date, no systematic testing solution has been proposed and visual inspection under microscopes is the most common test method [18], [19]. However, it suffers from low throughput, it is labor-intensive, and it requires expensive scopes, cameras, scanning stages, and complex vision-analysis software. Even skilled observers cannot systematically scan the entire chip at high resolution. More importantly, the fault coverage (percentage of detectable faults) obtained using visual inspection is inadequate: defects can easily escape detection and some defects are invisible under the microscope even at high magnification. For example:

1) valves cannot close completely. Two potential causes may lead to this defect: a) the membrane layer is too thick and b) flow channels are too tall;
2) poor bonding between channels: It could result in a short under pressure and these defects are undetectable through visual inspection.

Moreover, virtual inspection would over-test, and therefore leads to a unnecessary yield loss. For example:

1) *slight misalignment:* When valves are partially misaligned with underlying channels, the chip could still be functional and must be assessed with functional tests;
2) *debris trapped on different layers:* It may not affect functionality but a chip with debris on different layers may be classified as a defective chip by visual inspection.

Therefore, an automated functional test is necessary for mass adoption of PDMS microfluidic technology because it can stimulate the working environment and detect all defects which can cause faulty behaviors in the usage of these devices.

In this paper, we present the first approach for automated functional test of flow-based microfluidic biochips that use membrane-based valves for flow control. The proposed test technique infers the internal valve conditions from external pressure sensors by measuring the pressure in microchannels. Based on a behavioral abstraction of physical defects in microchannels and valves, the flow paths and flow control in the microfluidic device are modeled as a logic circuit composed of Boolean gates, which allows us to carry out test generation using standard ATPG tools. The tests derived using the logic circuit model are then mapped to fluidic operations involving pumps and pressure sensors in the biochip. Feedback from pressure sensors can be compared to expected responses based on the logic circuit model, whereby the types and positions of defects are identified. We also discuss the application of this test technique to biochips that use "valve compression" to reduce the number of valves for large designs. We describe the test-application setup for realistic scenarios and provide experimental demonstrations for two fabricated chips.

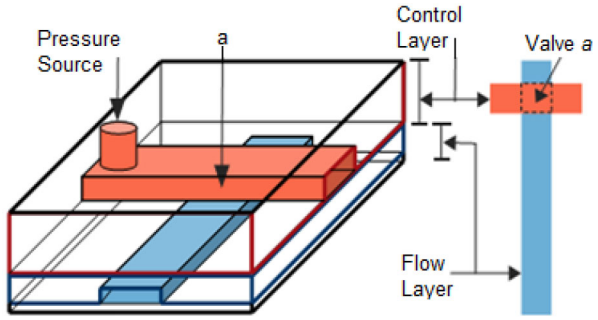


Fig. 1. Schematic of a two-layer flow-based biochip.

The rest of paper is organized as follows. Section II provides an overview of a flow-based microfluidic biochip and its fabrication process. Section III presents a list of defects for these chips. We relate these defects to four basic fault models and observable errors. Section IV describes the proposed test method, including logic circuit abstraction and ATPG. A defect, according to its type and position, can be mapped to a behavior-level fault, and be associated with a primary input of the logic circuit model. In Section V, a real chip is utilized as an example to show the procedures of logic circuit modeling and test pattern generation. Section VI expands the proposed fault modeling and testing strategy by addressing several practical concerns. In Section VII, a test-application and measurement system is designed for laboratory use, and two large-scale biochips are used for experimental demonstration of the proposed testing technique. Finally, conclusions are drawn in Section VIII.

## II. Flow-Based Microfluidic Biochips and Fabrication Method

A flow-based microfluidic biochip utilizes thousands of on-chip microvalves to manipulate pressure-driven flows in a complex network of etched microchannels. A basic microfluidic device is composed of two elastomer layers, and each layer has its own channel networks (Fig. 1). A flexible membrane, working as a micro-valve, is formed at the overlapping area between channels of the two layers. Biochemical fluids are carried in one layer (flow layer), and the other layer provides the pressure to deflect membrane valves into the flow channels and block fluidic flow (control layer). Channels in both layers are connected to an external pressure source, which generates the pressure to drive liquid flows and push-down membrane valves [5], [21].

This double-layer structure is fabricated by a technique called multilayer soft photolithography. Microfluidic network patterns are printed on silicon wafers by lithography. Two patterned wafers are made. They are used as molds for the control layer and flow layer, separately. Next, PDMS mixture is spun on the wafer mold to form a thin layer. After hard baking at 80 °C, the PDMS material changes to an elastomer with identical patterns of molds. Holes can be punched at this time to access the control and flow channels. After the control layer and flow layer are fabricated, they are removed from their molds and aligned together. The last step is to bake both layers

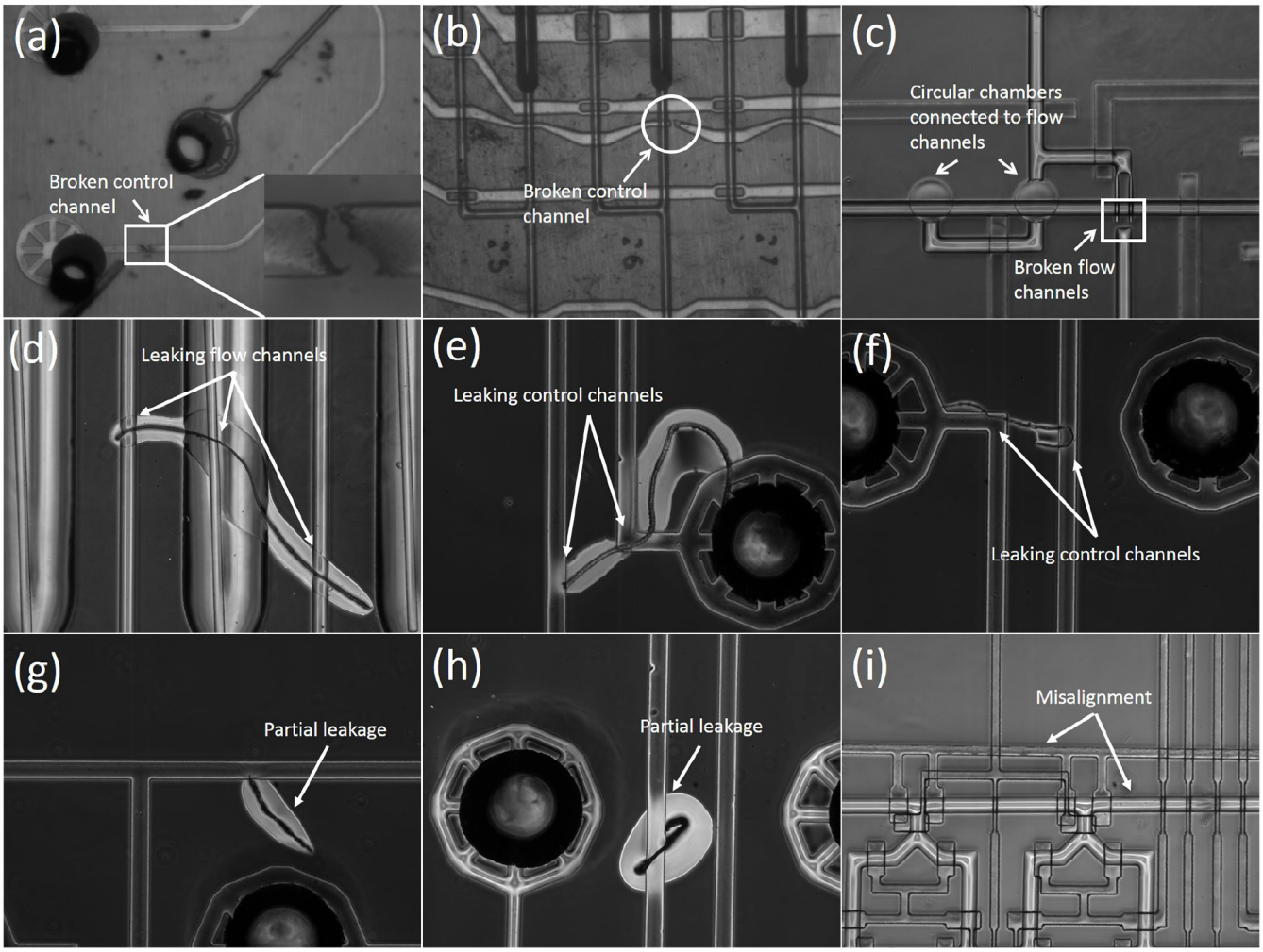


Fig. 2. Images of some typical visible defects in a fabricated flow-based microfluidic biochip. (a) Defect in the control layer. (b) Another defect in the control layer. (c) Defective flow channels. (d) Leaking flow channels. (e) Another example of leakage in a flow channel. (f) More leaky flow channels. (g) Partial leakage. (h) Another example of partial leakage. (i) Example of misalignment.

for bonding, which forms a bulk with complicated two-layer channel networks internal to it [3], [22].

## III. Defects and Fault Modeling

Defects in a flow-based microfluidic biochip can be attributed to fabrication steps and environmental reasons such as imperfections in molds, pollutants, bubbles in PDMS gel, and failure in hard baking. Furthermore, as feature sizes are scaled down, the sizes of and distances between micro-channels are reduced in order to achieve higher degrees of microfluidic integration. This increasing density raises the likelihood of defects. Some typical defects are listed below.

1) *Block:* Microchannels may be disconnected, blocked, or in some cases, even missing. Fig. 2(a)–(c) shows some examples of block defects in fabricated microfluidic devices. The potential causes are environmental particles or imperfect silicon wafer mold.
2) *Leak:* Some defective spots on the wall can connect independent micro-channels. The flows in either of them infiltrate into the other channel and the resulting cross-contamination can be catastrophic. It has been reported in [23] that the probability of a leaked channel pair increases as the length of the channels increases. It is higher if the distance between parallel channels decreases, and is less for channels that do not run in parallel. Fig. 2(d)–(f) shows some examples of leak defects caused by fiber pollutant in fabricated microfluidic devices. Moreover, some partial leak defects are shown in Fig. 2(g) and (h). These defective spots might become fully leakage when high pressure is injected into the channels.
3) *Misalignment:* Control layer and flow layer are misaligned (Fig. 2(i)). As a result, membrane valves either cannot be closed or are not even formed. The corresponding faulty behavior is similar to that of a block in the control channels.
4) *Faulty Pumps:* Pumps with defects fail to generate pressure when actuated. The faulty behavior here is similar to that for block; it interrupts the transmission of pressure.
5) *Degradation of Valves:* The membranes of valves might lose their flexibilities or even be perforated after a large number of operations. A consequence of this defect is that the valves cannot seal flow channels.
6) *Dimensional Errors:* The fabricated microchannels might be too narrow in comparison to the designed dimensions.

TABLE I
FAULTY BEHAVIOR DUE TO DEFECTS IN THE TWO LAYERS

| | Flow Layer | Control Layer |
|---|---|---|
| Block | Fluid flow cannot go through the obstacle inside channel so transport is blocked. | Pressure cannot reach the flexible membrane, which prevents the corresponding valve from closing. |
| Leak | Fluid flow permeates the adjacent microchannels. | Control channels of two independent valves are unintentionally connected. Pressure on either valve activates both. |

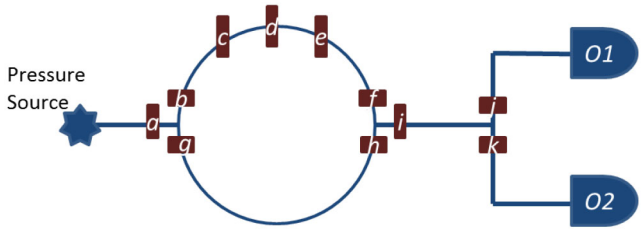


Fig. 3. Layout of a simple microfluidic chip with a mixer (the circle) and a branch. The lines indicate flow channels. Rectangles indicate the positions of valves, which are connected to pumps via control channels (not shown in the figure). *O1* and *O2* are outlet ports.

The mismatch of height-to-width ratio may lead to a valve that cannot be closed; as a result, the flow cannot be stopped in flow channels underneath the valve.

Despite the complexity of flow-based microfluidic biochips, the consequence of the above defects can be described as either a block or a leak. While these two generic fault types (block and leak) can be observed in both layers, their respective faulty behaviors are different (Table I).

We next make the observation that the errors due to defects can be modeled in terms of faulty behaviors of valves. For example, a block in a flow channel can be modeled as a valve that cannot be opened (deactivated), while a block in a control channel can be represented by valves that cannot be closed (activated). Similar behavioral models can be defined for leaks.

Let us consider Fig. 3 as an example and consider the following defects.

1) *Block in Flow Channels:* A block defect in the flow channel between valves *g* and *h* (the bottom semicircle of the mixer) leads to the behavior that valve *g* cannot be deactivated. (A valve and the channels connected to it are considered to be a single entity.)
2) *Block in Control Channels:* Pressurized air cannot reach the flexible membrane to seal the flow channel if a block defect exists in the control channel. In this case, valve *g* cannot be activated.
3) *Leak in Flow Channels:* Similar to a bridge (short) fault in integrated circuits, if a leak occurs between flow channels *g*-*h* and *b*-*c*, the liquid in channel *g*-*h* infiltrates channel *b*-*c*.
4) *Leak in Control Channels:* If a leak occurs between the control channels of *c* and *h*, the two shorted valves effectively form one valve. When either valve is activated, both valve *c* and *h* are activated.

## IV. TESTING STRATEGY

For testing, feedback signals are needed to identify chip conditions. However, for flow-based microfluidic biochips, only inlets and outlets are available to communicate with the outside environment. Therefore, we use a test set-up where feedback is generated when pressure sensors are connected to the outlets and pumps are connected to the inlets. If there is a path between pump sources (inlets) and pressure sensors (outlets), pressure sensors at the outlets detect a high pressure generated by the pumps. The measured high pressure is defined as output "1." If all routes between inlets and outlets are blocked, pressure sensors cannot sense the high pressure injected by the pumps. The absence of high pressure is defined as output "0." In flow-based biochips, all ports are physically identical, regardless of the functional classification of inlets and outlets. During testing, only one of ports in the flow layer is connected to a pressure source, while the rest are connected to pressure sensors.

TABLE II
LOGIC REPRESENTATION OF VALVE STATES AND PRESSURE RESPONSE

| Logic | Valve state | Valve condition | Pressure response |
|---|---|---|---|
| 1 | open | deactivated | high |
| 0 | closed | activated | low |

Similarly, a set of definitions for valve conditions is formulated. A "1" at a valve means that the valve is deactivated, i.e., low pressure in the control channel, while "0" indicates that the valve is activated, i.e., high pressure in the control channel. Table II connects the logic representation of valve states to the corresponding pressure response.

A binary pattern, also known as a test vector, is applied to all valves to set their open/close states. The actual responses of pressure sensors are compared to the expected responses. The microfluidic biochip is considered good if the two sets of responses match.

Table III illustrates the test strategy to target the faults in Table I for the design in Fig. 3. The test effectiveness depends on the quality of test patterns. As expected, the more complicated the microfluidic biochip structure is, the harder it is to determine a test pattern set that covers every fault type for each valve and channel. Therefore, it is necessary to further abstract defects and microfluidic structures to facilitate automatic test-vector generation.

Recall that defects in both flow channels and control channels can be modeled as the faulty behavior of a valve. Furthermore, a binary logic framework can be defined whereby an activate valve and a deactivate valve can be defined as logic "0" and "1," respectively. Hence, Table IV defines behavioral-level fault models for a flow-based microfluidic biochip.

TABLE III
TESTING STRATEGY FOR DIFFERENT KINDS OF FAULTS

| | Flow Channel | Control Channel |
|---|---|---|
| Block | Position: *g-h*. Both valves g and h are deactivated to form a route *inlet-a-g-h-i-k-O2*. If the output at *O2* is "0", the defect is detected. | Position: valve *h*. The block in control layer prevents valve from closing. Deactivate valve *a, g, i, k* and *O2* but activate the rest, including valve h. If *O2* is "1", the defect is detected. |
| Leak | Position: between *b-c* & *g-h*. Deactivate valve *a, b, h, i* and *k*. If high pressure is sensed at *O2*, the leaking defect is detected. | Position: valve *f* & *h*. Turn on valve *a, g, h, i, k* but activate *f*. If there is a leakage, high pressure in control channel *f* will activate valve *h* and therefore block route. |

TABLE IV
BEHAVIORAL-LEVEL FAULT MODEL FOR FLOW-BASED BIOCHIPS

| | Flow Layer | Control Layer |
|---|---|---|
| Block | stuck-at-0 | stuck-at-1 |
| Leak | OR bridge (1-dominant ) | AND bridge (0-dominant ) |

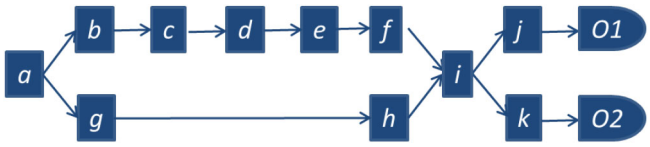


Fig. 4. Schematic of a valve network corresponding to Fig. 3. It can represent all interconnection relationships between channels and valves. Joint "*a*" not only represents valve "*a*" and its downstream flow channels, but also the on/off state of the fluid-injection pump.

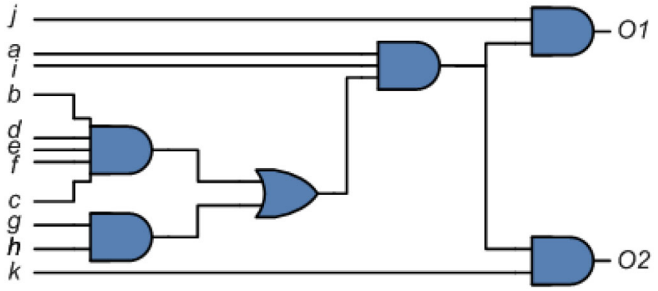


Fig. 5. Logic circuit model of the biochip shown in Fig. 3.

According to valve-based fault analysis, all types of defects occurring in both control channels and flow channels can be mapped to a specific behavioral-level fault at a valve. Such a classification simplifies the test problem for a 3-D structure to that for a 2-D design. It also simplifies test generation for chips with complicated networks of channels and valves.

For ease of description and analysis of biochip channel networks, we develop a discretized schematic of a valve network in place of a continuous fluid-flow topology. Fig. 4 illustrates an example for the design of Fig. 3. Logic relationships that define flow-based biochips can be inferred from this schematic, e.g., valve *b* is serially connected to valve *c, d, e*, and *f*. Therefore, either of these valves can potentially block the route, i.e., there is an "AND" logic relationship among them. On the other hand, routes *b-f* and *g-h* are in parallel, hence the activation of either of the two routes can lead to output "1," i.e., high pressure sensed by the corresponding pressure sensor. There is an "OR" logic relationship between them. We can thereby further abstract flow-based biochips from the intermediate schematic representative of valve networks to valve-based logic gate circuit diagrams, as shown in Fig. 5, whose logic expression is $\{O1, O2\} = \{j, k\} \cdot a \cdot i \cdot (b \cdot c \cdot d \cdot e \cdot f + g \cdot h)$. The primary inputs are nodes in the schematic of Fig. 4.

We list below two important attributes of the logic circuit model.

1) Only primary inputs (valves) and outputs (pressure sensors) have physical meaning. All other circuit connections are used to represent logical relationships. As a result, we only need to target faults at the primary inputs of this circuit.
2) A series connection of valves in a flow route is mapped to an AND gate. On the other hand, a parallel connection of valves is mapped to an OR gate.

Therefore, based on Fig. 5 and Table IV, we note that a physical defect in a flow-based biochip can be mapped to a fault at a primary input of a logic circuit. For example, to target a block defect in flow channel *g-h*, we can first map this defect to a stuck-at-0 fault according to Table IV, and after that this fault is associated with the primary input *g* in the logic circuit model (Fig. 5). Similarly, a leak defect between valve *f* and *h* can be represented by an AND bridge fault between primary inputs *f* and *h* of Fig. 5. Based on the logic circuit model, we can readily determine the actual (with faults) and expected (fault-free) responses of pressure sensors and therefore accelerate the search for test stimuli. If the actual outputs are different from the expected ones, we can not only conclude that the chip is faulty, but also infer the positions and types of defects. The logic circuit model therefore provides a concise representation and we can use ATPG algorithms and tools for test-stimuli generation. We can reduce the number of pressure sensors at the cost of more test patterns and test time. Note that this test method involves hooking up control lines and sensors to the chip, which may take considerable set-up time in a lab. However, in an industrial setting, acrylic jigs can be built for each chip manufactured to eliminate setup time. These jigs will have all the ports and sensors preconnected. All one has to do is to align the jig to the chip and apply pressure so that the connection is airtight.

Recall that each valve node in the schematic of the valve network (or the primary input of the logic circuit model) represents not only the valve itself, but also its downstream flow channel. Therefore, we need to study how valve compression affects the logic model and the test generation method.

1) *Valve Sharing:* If two valves have the same synchronized behavior, i.e., the same tempo in opening and closing,

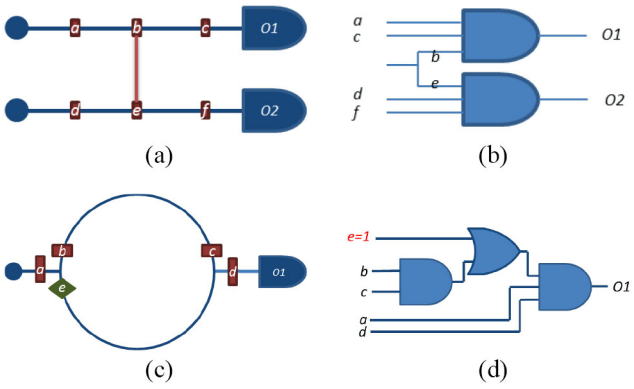


Fig. 6. (a) Valve sharing. Valve *b* and *e* share the same control channel and pump. (b) Logic model for (a). Note that input *b* and *e* are connected together. Faults might occur at both fanin branches. (c) Valve *e* is canceled so that the bottom half of mixer does not have the faults of the control layer (stuck-at-1 and AND bridge). (d) Logic model for (c). Although valve *e* does not exist, a fictitious stuck-at-1 primary input is added to represent the corresponding flow channel.

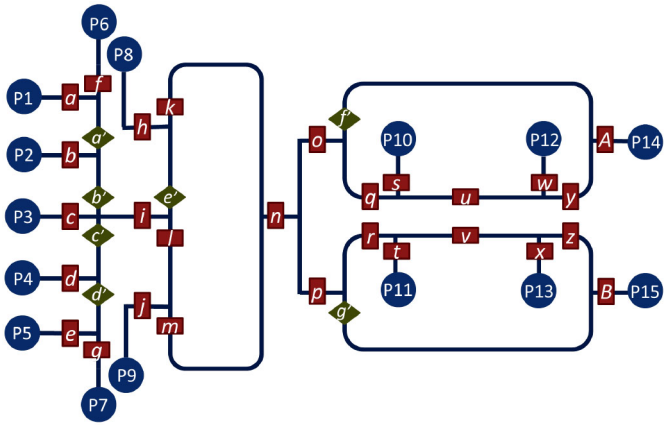


Fig. 7. Layout of a fabricated flow-based microfluidic biochip [20]. Rectangles indicate the positions of valves, which are connected to pumps via control channels (not shown in the figure). Diamonds indicate the positions of seven fictitious valves (*a'-g'*). P1–P15 are fluid inlets and outlets in the flow layer, which are physically identical and therefore can be connected to either pumps or pressure sensors according to the test plan.

they can be designed to share a control line and a pump, e.g., valve *b*-*e* in Fig. 6(a). Correspondingly, in the logic circuit model, their equivalent primary inputs are connected together [see Fig. 6(b)]. Note that both fanin branches can be faulty, hence they need to be targeted in test generation.

2) *Valve Cancellation:* If a flow channel permanently carries fluid for a bioassay, the valve that controls it can be canceled (or deleted from the model). However, in the logic circuit model, a fictitious stuck-at-1 primary input needs to be inserted to indicate this flow channel. Moreover, due to the absence of the control channel, the number of faulty types of this fictitious input is reduced from four to two, i.e., stuck-at-0 (block in the flow channel) and OR-bridge (leak in the flow channel) [see Fig. 6(c) and (d)].

## V. Applications to Fabricated Biochip

This section illustrates the procedure of circuit modeling and test pattern generation for a fabricated flow-based microfluidic biochip [20]. The chip is first modeled as a logic circuit using the method discussed in Section IV, and after that test patterns are generated by TetraMAX, an ATPG tool from Synopsys. A total of 30 test patterns are needed to test 99 faults. All faults are detected; hence the fault coverage is 100% [24].

### A. ChIP Biochip and Logic Circuit Model

The flow-based biochip used in this example (Fig. 7) is designed for chromatin immunoprecipitation (ChIP), an assay which analyzes DNA-protein interactions [20]. This biochip contains 28 valves and 15 ports in the flow layer. The corresponding valve logic circuit model is shown in Fig. 8, in which we add seven fictitious stuck-at-1 faults on primary inputs (*a*'-*g*') to denote canceled valves.

In an actual application, i.e., in functional mode, P1–P5 are used as inlets where reagents are injected, while P6–P15 are used as outlets. However, for the purpose of testing, since

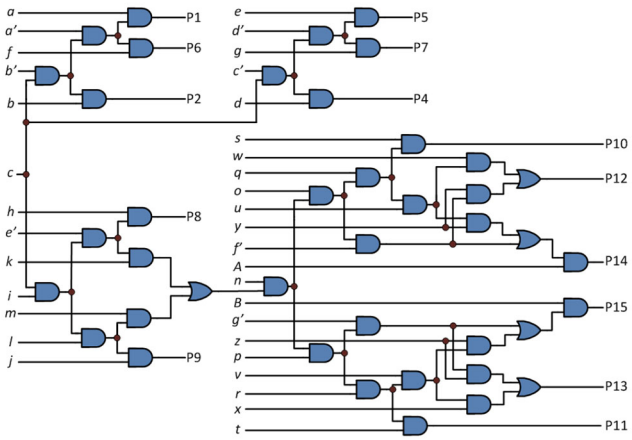


Fig. 8. Logic circuit model of the layout in Fig. 7.

inlets and outlets are physically identical, we can randomly select any one or multiple ports as "inlets." In this example, only P3 is connected to a pump. Each of the other ports is connected to an individual pressure sensor. The corresponding logic circuit model is presented in Fig. 8. In other scenarios where pumps are assigned to different ports, the logic models will be different and will need to be developed appropriately.

### B. Test-Pattern Generation and Results

A commercial ATPG tool, TetraMAX from Synopsys, is utilized to generate test patterns. First, a Verilog file is created to describe the logic circuit in Fig. 8. Also, a fault list is set up to restrict the locations of faults (primary inputs only). An optimized set of test patterns is generated in only a few seconds of CPU time, and the ATPG tool reports the number of test patterns, fault coverage, and lists of detectable and undetectable faults. Using this report, biochip engineers can refine the layout to avoid the occurrence of undetectable faults.

We first discuss the testing of stuck-at faults in the logic circuit, which model block defects in the biochip. Stuck-at-0

TABLE V
LIST OF 30 TEST PATTERNS AND THEIR CORRESPONDING EXPECTED FAULT-FREE RESPONSES FOR ACHIEVING 100% FAULT COVERAGE. A TEST PATTERN IS ARRANGED IN ALPHABETICAL ORDER (*a–z, A, B*); EXPECTED RESPONSE IS ARRANGED IN THE ORDER OF P1, P2, P4–P15. THE "DETECTED FAULTS" COLUMN SHOWS THE NUMBER OF FAULTS THAT EACH TEST PATTERN CAN DETECT

| Stuck-at Faults | | | | Bridging Faults | | | |
|---|---|---|---|---|---|---|---|
| | Test Pattern | Expected Response | Detected Faults | | Test Pattern | Expected Response | |
| 1 | 1111010101 1000100101 10101000 | 1110100000 0000 | 12 | 1 | 1110111111 1101101010 10101110 | 1101111110 1010 | |
| 2 | 0111001010 0101110101 00010011 | 0110010000 0000 | 10 | 2 | 1110011111 1111100110 01010111 | 1100111100 0010 | |
| 3 | 1110011110 1001111001 11001111 | 1100111000 1111 | 13 | 3 | 1011110010 1011010101 10000101 | 1011100001 0101 | |
| 4 | 1110010011 1011100011 10010011 | 1100100000 0010 | 4 | 4 | 1011000111 1101111001 11101100 | 1010001100 1100 | |
| 5 | 0110100110 1011101000 11110100 | 0101001000 1000 | 5 | 5 | 1010011110 1011110100 01011000 | 1000111000 1100 | |
| 6 | 1111011010 1001111101 11111000 | 1110110001 1100 | 5 | 6 | 1110001110 1001011100 10111000 | 1100011000 0000 | |
| 7 | 0010101010 1101101011 01011001 | 0001010010 1000 | 2 | 7 | 0010111010 1101101100 10110000 | 0001110000 1000 | |
| 8 | 1010011111 1101010100 10011100 | 1000111100 0100 | 4 | 8 | 1011011110 1111111110 01100100 | 1010111010 0100 | |
| 9 | 0010011010 1101011101 00100010 | 0000110001 0000 | 1 | 9 | 0010010011 1111011011 10000100 | 0000100100 0100 | |
| 10 | 0011010011 0111110100 00000011 | 0010100100 0011 | 1 | 10 | 1111100111 0011111100 01000001 | 1111001000 0000 | |
| 11 | 0100101011 0101010100 01001101 | 0000000000 0000 | 1 | 11 | 1110110010 1001111110 00100000 | 1101100010 0000 | |
| 12 | 1010100111 1000111000 01101011 | 1001001000 0000 | 1 | 12 | 1011111000 1101000111 00001110 | 1011110000 0000 | |
| 13 | 1011010011 1101111100 00100001 | 1010100100 0001 | 1 | 13 | 1011001111 0101101010 11100001 | 1010011100 0000 | |
| 14 | 1110001010 1101110100 10011001 | 1100010000 1001 | 1 | 14 | 0111100110 0111111110 01110000 | 0111001010 0100 | |
| 15 | 1010011011 1111111010 11000100 | 1000110110 0100 | 1 | | | | |
| 16 | 1011110111 1011110100 11001000 | 1011101000 1000 | 1 | | | | |

and stuck-at-1 are considered for all primary inputs, except the seven fictitious inputs, where only stuck-at-0 faults exist. The ATPG fault list therefore contains $28 \times 2 + 7 = 63$ faults. ATPG results show that 16 tests are sufficient to cover all these stuck-at faults. The test patterns are listed in Table V. The length of each expected response is 14 bits, representing P1, P2, and P4–P15 since P3 is connected to a pump. The length of the test patterns is 28 bits, representing the 28 valves in the biochip. For example, the binary vector for the first pattern indicates that Valves 5, 7, 9, 12–14, 16, 17, 19, 22, 24, 26–28 should be closed (activated) and all other valves should be open (deactivated).

Next, we discuss the testing of bridging faults in the logic model, which correspond to leak defects in the biochip. We note from Section III that leakage can only involve channel pairs that are parallel and close to each other. It is therefore unnecessary to consider all channel pairs in the layout. We can generate a list of likely leak faults to reduce the size of the resulting fault list and test patterns. Based on this criterion, only the following channel pairs appear in the fault list: 1) channel pairs *q-r, u-v, y-z, i-h, i-j, k-h, j-m, h-f*, and *j-g* might leak in the control layer and flow layer, hence OR bridges and AND bridges are inserted at those locations; 2) control channels of valves *i, j, g* are close to each other, hence AND bridges are inserted into the fault list for these three valves; 3) for fictitious channel pairs of *h-a'*, *j-e'*, only OR bridges are possible. Finally, there are 36 bridging faults in the fault list and ATPG generates 14 test vectors to detect all of them (Table V).

As discussed above, all the candidate logic faults can be detected by 30 test patterns. By activating and deactivating the pumps connected to each valve, the opening and closing of 28 valves are controlled, hence the 30 test patterns can be applied one after the other. The feedback to test patterns from pressure sensors are compared to expected fault-free responses. If the biochip under test passes all 30 measurements, we conclude that the chip is fault-free. Otherwise, the chip is faulty.

## VI. OTHER PRACTICAL CONCERNS

This section expands the proposed fault modeling and testing strategy by addressing three practical concerns—test cost, dynamic and multiple faults, and potential solutions for the testing of dynamic faults.

### A. Test Cost

Test cost is another concern for the motivation of the proposed test technique. Although flow-based biochips are for one-time use and very cheap, the main cost due to a faulty chip is not the chip itself, but the wastage of expensive samples, reagents, and the users time. Moreover, faulty chips may lead to misdiagnosis, which is completely unacceptable and must be prevented. Therefore, robust post-fabrication testing methods for flow-based biochips are indeed necessary. Additionally, the cost of the testing system is very low. The only requirements are several off-the-shelf pressure sensors. A typical silicon pressure sensor, which we used in the demonstration experiments, costs only $35 [25]. The total cost of the testing system used in this paper is less than $1000.

### B. Dynamic Faults

The defects discussed in this paper, including blockage, leakage, misalignment, faulty pumps, and degradation of vales, can be categorized as being static. The consequence of static defects can be described as either a block or a leak. In addition to static defects, some defects may lead to malfunctions in certain scenarios. We call them dynamic defects. Instead of completely cutting off flow, dynamic defects increase the hydrodynamic resistance, and consequentially, decelerate pressure propagation in the microchannels. Some typical dynamic defects are partial block, coarse channel surface, erroneous channel dimensions, etc. The detection of dynamic defects cannot be guaranteed by the proposed testing set-up because the feedback of a pressure sensor is either "1" or "0." Note, however, that dynamic defects can be viewed as soft defects.

They can be overcame if: 1) the execution time of each fluidic operation includes adequate slack or 2) the output pressure of pressure sources is sufficiently high. The testing method proposed in this paper is a functional test that can mimic the working environment, and detect all defects that can lead to errors during the usage of these devices. Hence, even if there are dynamic defects in the chips under test, they will not cause malfunctions if the chips pass the test under the same working conditions.

Furthermore, we can effectively detect dynamic defects by improving the proposed testing strategy. Note that the increase in hydrodynamic resistance leads to a deceleration in pressure propagation. Hence, we can detect a dynamic defect by: 1) producing an appropriate pressure change at a primary output and 2) sampling the pressure in the microchannels multiple times to monitor the pressure change. According to our experimental results, the pressure change in three seconds in a closed microchannel should be smaller than 0.15 psi, while that in an open microchannel should be larger than 1.1 psi. More details regarding the demo systems and experimental measurement procedures are described in Section VII (Figs. 11 and 12). Note that a closed microchannel can result from either a closed valve or a complete blockage defect. Therefore, if the pressure change is slow, i.e., in the range of 0.15–1.1 psi in 3 s, we can make a conclusion that there are dynamic defects in the chip. For example, partially closed valves can be detected if the pressure increases slowly when the faulty valve is closed. Partially disconnected microchannels and slightly misaligned channels can be detected if a slow pressure increase is observed.

### C. Multiple Faults

It is possible for a chip to contain multiple defects. In our method, each physical defect in the layout is mapped to a fault in the logic-circuit model. Hence, if a fault is masked by other faults in the logic-circuit model, we cannot detect the corresponding defects in the chip. However, research in circuit testing has demonstrated that masking of multiple stuck-at faults is rare in a combinational circuit; published work has shown that as high as 99.6 percent of faults can be detected regardless of the presence of other faults in a circuit with three or more primary outputs [26], [27]. Therefore, the single-fault model proposed in the paper is adequate.

## VII. Experiment Demonstration

In this section, experimental results are presented to evaluate the feasibility of the proposed test method. Next, the method is applied to two representative and fabricated flow-based microfluidic biochips. A physical test system is implemented to apply test patterns and measure test responses. Defects are successfully detected for both kinds of chips.

### A. Experiment Feasibility Demonstration

Water is commonly used as the flow medium in PDMS biochips. However, for the purpose of testing, water should be avoided because: 1) the flow rate of water is too low to register any significant pressure changes at the output and 2) water may remain in the channels after testing, and therefore cause contamination and interfere with on-chip chemistries. Thus, air must be used as the flow medium during testing, even though PDMS material is porous and therefore is permeable to air. The impact of air permeability of PDMS biochips on pressure transportation and detection will be discussed later.

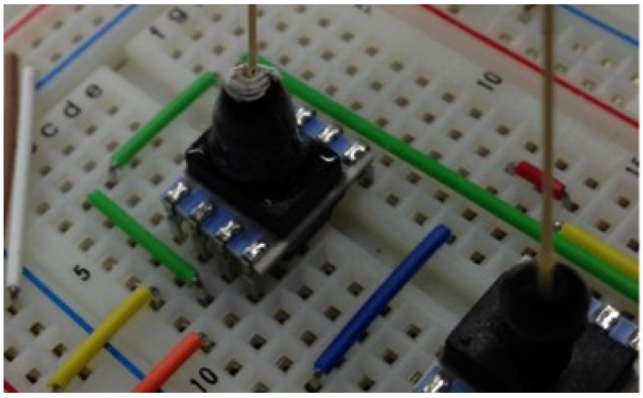

Fig. 9. Connections between pressure sensors and capillary tubing.

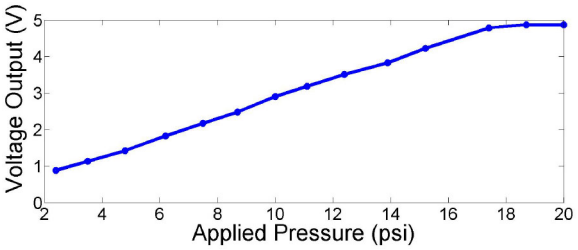


Fig. 10. Sensor readout for different applied pressure values.

To measure the pressure of a channel at the output, dead volume should be minimized and the connections must be airtight. To minimize dead volume, very thin capillary tubes are used to connect the chip output to the sensor. The other end of the tubing is directly plugged into the chip outlet. For an airtight connection, each connection between pressure sensors and capillary tubings should to be wrapped with PTFE tape first and then sealed with epoxy. Pressure sensors from Honeywell are used in our experiment (Part number: SSCDANT015PGAA3). The sensor is a piezo-resistive silicon sensor offering an analog voltage output for pressure range from 0 psi to 15 psi (pressure reference: atmospheric pressure). The sensors and the connections are shown in Fig. 9. Fig. 10 illustrates the relationship between applied pressure and the voltage output for the connection method used for the test set-up.

Due to the air permeability of PDMS, pressure in the channels tends to drop steadily when air flow is used for testing. This is important to note because the decrease of air pressure inside channels may interfere with signal detection and even lead to erroneous measurements. Fig. 11 presents the air pressure changes in a microchannel fabricated by PDMS materials, for which two cases are considered. High pressure and low pressure are injected for the two cases, respectively, and the channel is sealed by an activated valve and a pressure

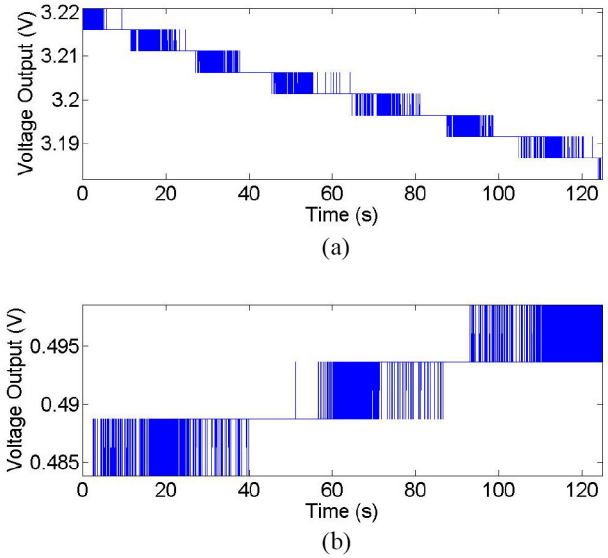


Fig. 11. Measured air pressure maintenance when a microchannel is sealed by an activated valve at one end and a pressure sensor at the other end. (a) High pressure is maintained in the microchannels. (b) Vacuum is maintained in the microchannels.

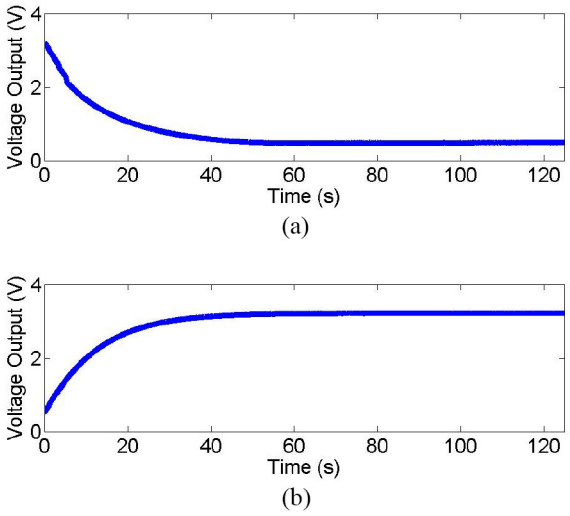


Fig. 12. Response over time of pressure sensors when microchannels are injected with low/high pressure. (a) Low pressure is injected. (b) High pressure is injected.

sensor at both ends. This figure indicates that air pressure can be maintained in a stable manner for at least one minute, which is much longer than the measurement time for each pattern. Moreover, it also demonstrates that a membrane valve can effectively seal air pressure in the flow channels. Accordingly, air is an eligible pressure medium for the purpose of testing in a flow-based microfluidic biochip fabricated by PDMS materials. In these experiments, the pressure pumps are set to 21 psi to push down membrane valves; the pressure source is set to 11 psi to inject high pressure signals into flow channels and a vacuum source is used for low pressure signals. These values are used in all the experiments reported in this paper.

### *B. Pattern Set-Up Time, Measurement Time, and Refresh Time*

In testing, valves must be opened or closed according to test patterns, and then pressures are measured through external pressure sensors. Typically, a large-scale flow-based microfluidic biochip needs hundreds of patterns for acceptable fault coverage. Therefore, shortening the execution time for each pattern is crucial for efficient testing.

In an ideal scenario, air pressure is evenly distributed in a channel. Thus, pressure changes should be detected once air is injected through a pressure source. Nevertheless, Fig. 12 indicates that there is a serious sensing delay (∼50 s) after high/low pressure is injected. According to the datasheet, the output values of pressure sensors can indicate changes at approximately every 1 ms. Hence, the sensing delay should be mainly attributed to the pressure propagation delay in the microchannels. In microfluidics, pressure and flow rate are analogous to electronic concepts of voltage and current respectively. Therefore, this pressure-propagation delay can be modeled as a ladder RC circuit model [28]. Pressure will dilate microchannels due to the flexibility of PDMS, i.e., the energy of compressed air will be transferred and stored as mechanical potential energy of channel walls. This energy storage can be modeled as a hydrodynamic capacitor. Similarly, the flux of air/water flow is restricted by microchannels. Hence, microchannels can be modeled as hydrodynamic resistors, whose resistance is linear in $l/w^2$ ($w$: cross section area of a microchannel; $l$: channel length) [29].

It has been shown that a valve is closed because high pressure in the control channels deflects the membrane valve and blocks flow channels. Just like pressure propagation delay in flow channels, pressure propagation in control channels also leads to a delay between the activation of a pressure pump and the complete closure of the corresponding valve. However, pressure sensors must not measure pressure in the flow channels until test patterns are completely set up. Therefore, a pattern set-up time is necessary to ensure that all valves are set to the expected conditions. Typically, the pattern set-up time is 3 s.

Fig. 12 shows that to determine whether the pressure in the flow channel is high or low, at least 50 s are needed until the pressure in the microchannels becomes stable. This is obviously an unacceptable lag time, especially for a large chip. To accelerate the sensing process, we can measure the dynamic pressure change instead of the static pressure: two pressure measurements are made sequentially after the test pattern is set. If the output of a pressure sensor increases, it can be inferred that there is a pathway between the pressure source and this sensor, i.e., the response of this sensor is "1"; Otherwise, if the readout of a pressure sensor does not change, it can be inferred that the pathway between the pressure source and this sensor are blocked, i.e., the response of this sensor is "0." Typically, the time interval between two measurements is set to 3 s (measurement time). According to Figs. 11 and 12, if the initial pressure in the channels is low, less than 0.03 V output difference, i.e., 0.15 psi pressure change, should be detected for a response of "0," and more than 0.25 V output difference, i.e., 1.1 psi pressure change,

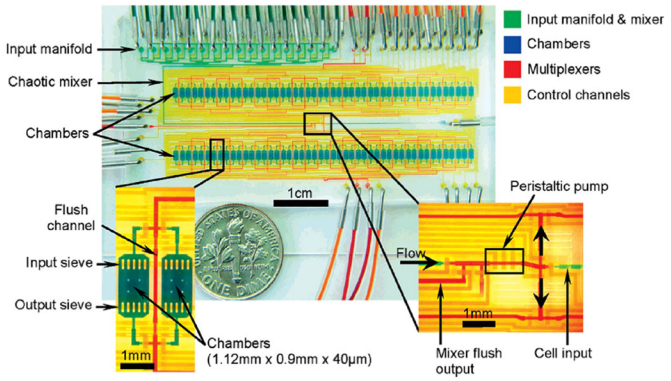


Fig. 13. Layout of the cell culture chip [30].

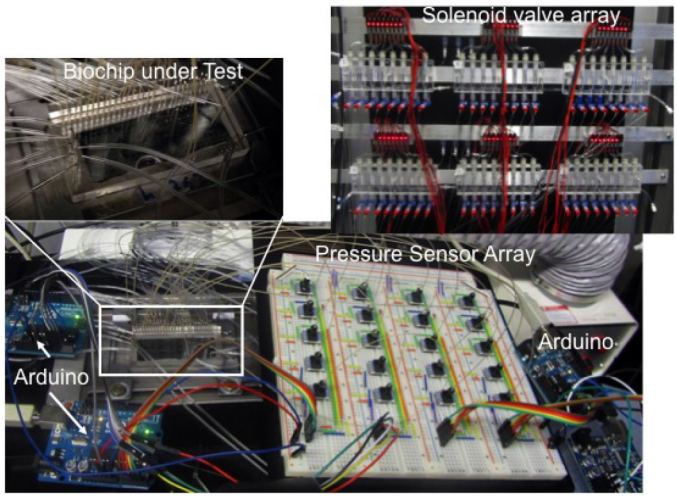


Fig. 14. Demo system for the testing of flow-based microfluidic biochips in the laboratory.

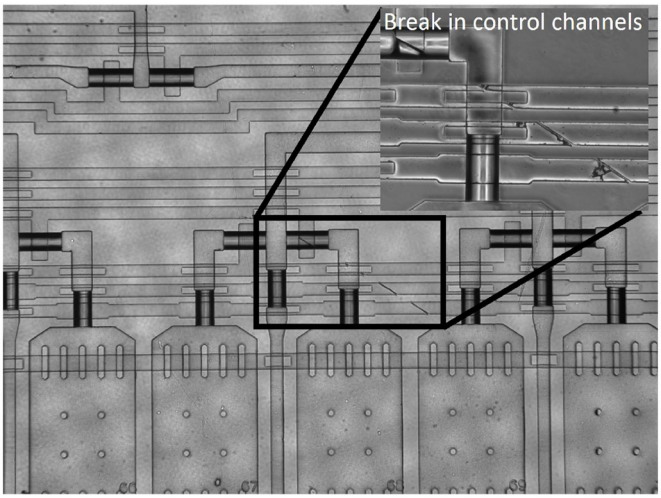


Fig. 15. Image of the faulty cell culture chip under test. The chip suffers from block defects in the control channels.

should be detected for a response of "1." Recall that dynamic defects decelerate pressure propagation in the microchannels. Hence, if the pressure change is in the range of 0.03–0.25 V under the same measurement conditions, we can make a conclusion that the pressure propagation in the microchannel is neither completely blocked nor transmitted freely, i.e., there are dynamic defects in the chip.

Furthermore, Fig. 12 demonstrates that the pressure will increase more slowly if pressure in the channel is high. Therefore, a low pressure is required so that sensors can detect a measurable change in a short period of time. In our experiments, after each pattern is executed, all valves are opened and a vacuum source is activated to keep the pressure in the channels at a low level. This "refresh" stage typically takes 3 s in our experiments.

In summary, it takes 9 s in total for the execution of each test pattern: 3 s for pattern set-up, 3 s for dynamic pressure measurement, and 3 s for pressure refresh.

### C. Experiment Demonstration I: Cell Culture Chip

The proposed testing approach is evaluated using a fabricated flow-based microfluidic biochip, whose layout is shown in Fig. 13 [30]. This chip can perform automated cell culture with 96 individually addressable culture chambers. It contains 720 valves, 24 ports in the flow layer, and 48 ports in the control layer. In this experiment, Port "Treat" is selected to be connected to a pressure source. After running ATPG for this chip, we obtain 82 test vectors for stuck-at faults and 10 vectors for bridging faults.

The demo test system used in the laboratory is shown in Fig. 14, where 48 solenoid valves are utilized to control pressure injection into control channels, i.e., the open/close of on-chip microvalves. Pressure sensors and their support circuits are integrated on a breadboard and are connected to ports of biochips through capillary tubing. Solenoid valves and pressure sensors are both individually controllable by MATLAB. After solenoid valves are set according to the test pattern (pattern set-up stage), pressure sensors measure the pressures changes in the flow channels (measurement stage), and then all valves open and a vacuum source ensures that there is vacuum in all the flow channels (refresh stage). Arduino microcontrollers are used to read the voltage outputs of pressure sensors and send the signals to MATLAB. A fault-free cell culture chip and a chip with blockage defect in the control channels (Fig. 15) are tested. For the fault-free chip, all sensor readouts match expected responses generated by ATPG; for the defective chip, the test failed because corresponding valves could not be opened.

Table VI shows average pressures and average pressure changes for different measurement time and refresh time. Average pressure in the chip becomes lower when refresh time is increased. Furthermore, the pressure changes grow larger as measurement time and refresh time increase. The reason for this behavior is that: 1) pressure changes accumulate with measurement time and 2) the refresh process keeps pressure in the biochip at a low level, therefore, pressure changes are rapid for sensors whose responses are "1."

Fig. 16 estimates the delay between pump actuation and valve closure. The target valves are the valves with the longest control channel because they suffer the most from pressure-propagation delay. Initially, all valves are open and vacuum is

TABLE VI
AVERAGE PRESSURES AND AVERAGE PRESSURE CHANGES IN CELL CULTURE CHIPS FOR DIFFERENT MEASUREMENT TIME AND REFRESH TIME. (a) AVERAGE PRESSURE (PSI). (b) AVERAGE PRESSURE CHANGES (PSI)

(a)

| Refresh Time (s) | Measurement Time (s) | | |
|---|---|---|---|
| | 1 | 2 | 3 |
| 1 | 3.93 | 5.06 | 5.74 |
| 3 | 1.81 | 2.62 | 3.25 |
| 6 | 0.88 | 1.31 | 1.78 |

(b)

| Refresh Time (s) | Measurement Time (s) | | |
|---|---|---|---|
| | 1 | 2 | 3 |
| 1 | 0.124 | 0.231 | 0.313 |
| 3 | 0.174 | 0.347 | 0.487 |
| 6 | 0.200 | 0.413 | 0.598 |

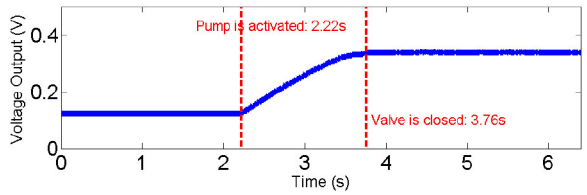


Fig. 16. Estimation of pattern set-up time. The valve-activation delay is $3.76 - 2.22 = 1.54$ s.

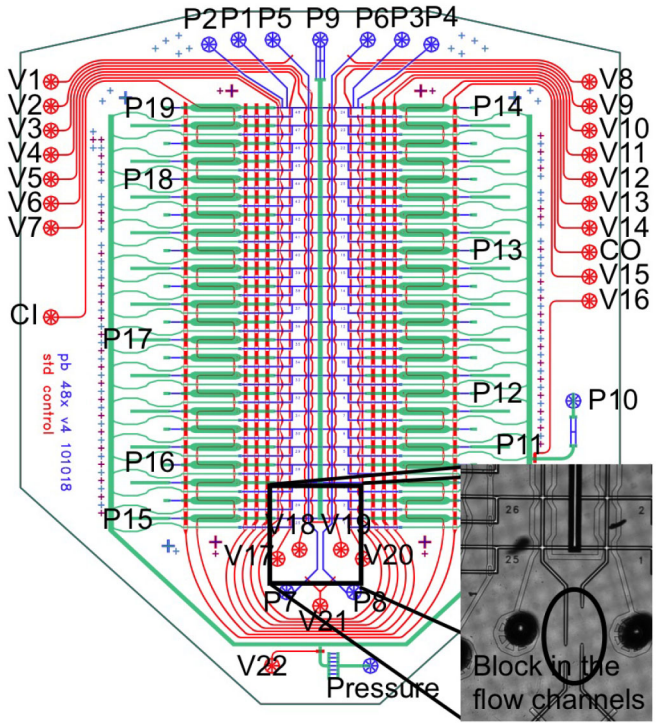


Fig. 17. Layout of the WGA chip [31]. The faulty chip under test suffers from block defects in the flow channels, which are zoomed into and shown as well.

maintained in all flow channels. Then the pump connected to target valves are activated and at the same time, high pressure is injected into flow channels. Due to the pressure-propagation delay, pressure in the flow channels keeps increasing until valves are completely closed. Thus, the valve actuation delay (1.5 s) is obtained in Fig. 16 and the pattern (3 s in this experiment) must be longer than this delay.

### *D. Experiment Demonstration II: WGA Chip*

The second flow-based microfluidic biochip tested in our experiments is designed for whole genome amplification (WGA) [31]. The chip contains 235 valves, nine ports in the flow layers, and 23 ports in the control channels. The chip layout is shown in Fig. 17. Control channels are shown in red. The blue and green flow channels have different dimensions. Therefore, their connections can be tested be assign a pressure source at either of them and a pressure sensor at the other. The rest of chip can be tested by 12 test vectors, which are shown in Table VII. The port "Pressure" is connected to a pressure source.

A fault-free chip and a defective chip with block defects shown in Fig. 17 are tested. As expected, all sensor feedback data match the expected responses for the fault-free chip. In the case of the defective chip, pressure sensors report errors at Test Pattern 10 and 11 due to the block defects.

Table VIII shows average pressure values and average pressure changes for all 18 patterns for the fault-free chip. As anticipated, an increase in the measurement time and refresh time can increase the pressure changes at the cost of longer testing time.

TABLE VII
LIST OF THE 12 TEST PATTERNS FOR WGA CHIPS AND THEIR CORRESPONDING EXPECTED FAULT-FREE RESPONSES. THE NUMBER OF TEST PATTERNS HAVE BEEN OPTIMIZED BY ATPG TOOLS TO MINIMIZE TESTING TIME. A TEST PATTERN IS ARRANGED IN THE ORDER V1–V22; AN EXPECTED RESPONSE IS ARRANGED IN THE ORDER P1–P19

| | Test Pattern | Expected Response |
|---|---|---|
| 1 | 11111 11111 11111 11111 10 | 00000 00000 00000 0000 |
| 2 | 01011 01100 10111 10011 01 | 00000 00001 00000 0000 |
| 3 | 10110 01111 11110 01111 11 | 00000 00000 00000 0000 |
| 4 | 10111 11011 11101 01111 01 | 11000 00010 00000 0000 |
| 5 | 01011 11111 01110 00011 01 | 00001 10000 00000 0000 |
| 6 | 11011 01011 11011 01111 11 | 00000 00000 00000 0000 |
| 7 | 01011 00111 11111 01111 11 | 00000 00000 00000 0000 |
| 8 | 11001 01011 01111 01010 11 | 00000 00000 00000 0000 |
| 9 | 01011 01111 10111 01100 11 | 00000 00000 00000 0000 |
| 10 | 10110 11010 11111 00101 11 | 00000 01110 11110 0000 |
| 11 | 11111 11111 11111 01111 11 | 11111 11110 11111 1111 |
| 12 | 11111 01111 11111 01111 11 | 00000 00000 00000 0000 |

TABLE VIII
AVERAGE PRESSURES AND AVERAGE PRESSURE CHANGES IN WGA CHIPS FOR DIFFERENT MEASUREMENT TIME AND REFRESH TIME. (a) AVERAGE PRESSURE (PSI). (b) AVERAGE PRESSURE CHANGES (PSI)

(a)

| Refresh Time (s) | Measurement Time (s) | | |
|---|---|---|---|
| | 1 | 3 | 6 |
| 1 | 1.04 | 1.60 | 1.87 |
| 3 | 0.99 | 1.17 | 1.39 |
| 6 | 0.63 | 1.06 | 1.11 |

(b)

| Refresh Time (s) | Measurement Time (s) | | |
|---|---|---|---|
| | 1 | 3 | 6 |
| 1 | 0.085 | 0.213 | 0.382 |
| 3 | 0.091 | 0.234 | 0.417 |
| 6 | 0.091 | 0.247 | 0.463 |

## VIII. CONCLUSION

An automated functional test method has been described for targeting blocking and leakage defects in flow-based microfluidic biochips. The proposed test technique is based on a behavioral abstraction of physical defects in microchannels and valves. The flow paths and flow control in the microfluidic device have been modeled as a logic circuit composed of Boolean gates, which allows us to carry out test generation

using standard ATPG tools. Only primary inputs in the logic circuit model, which correspond to valves in the biochip, need to be targeted during test generation. The 0–1 tests derived using the logic circuit model can be easily mapped to fluidic operations involving pumps and pressure sensors in the biochip. For example, a logic value of "1" ("0") at a primary input in the circuit model indicates that the corresponding valve is open (closed). Feedback from pressure sensors can be compared to expected responses based on the logic circuit model, whereby the types and positions of defects are identified. An experimental test setup has been developed and demonstrations have been presented for two fabricated biochips.

## ACKNOWLEDGMENT

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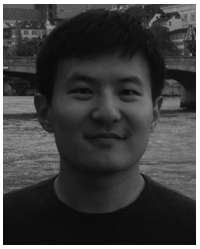

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