Lab on a Chip

RSC Publishing

PAPER

View Article Online
View Journal | View Issue

Cite this: *Lab Chip*, 2013, **13**, 1911

Microfluidic serial digital to analog pressure converter for arbitrary pressure generation and contamination-free flow control†

Feiqiao Yu,[ab] Mark A. Horowitz[b] and Stephen R. Quake*[a]

Multilayer microfluidics based on PDMS (polydimethylsiloxane) soft lithography have offered parallelism and integration for biological and chemical sciences, where reduction in reaction volume and consistency of controlled variables across experiments translate into reduced cost, increased quantity and quality of data. One issue with push up or push down microfluidic control concept is the inability to provide multiple control pressures without adding more complex and expensive external pressure controls. We present here a microfluidic serial DAC (Digital to Analog Converter) that can be integrated with any PDMS device to expand the device's functionality by effectively adding an on-chip pressure regulator. The microfluidic serial DAC can be used with any incompressible fluids and operates in a similar fashion compared to an electronic serial DAC. It can be easily incorporated into any existing multilayer microfluidic devices, and the output pressure that the device generates could be held for extensive times. We explore in this paper various factors that affect resolution, speed, and linearity of the DAC output. As an application, we demonstrate microfluidic DAC's ability for on-chip manipulation of flow resistance when integrated with a simple flow network. In addition, we illustrate an added advantage of using the microfluidic serial DAC in preventing back flow and possible contamination.

Received 19th December 2012,
Accepted 4th March 2013

DOI: 10.1039/c3lc41394b

www.rsc.org/loc

Introduction

Microfluidic devices allow high throughput, precise manipulation of nanoliter volumes of liquids and have recently led the rapid advancement of experimental methods in biological and chemical sciences. Allowing control and monitoring of chemical reactions and biological processes at single cell or even single molecule resolution, these devices have created techniques such as digital PCR,[1–4] digital MDA (Multiple Displacement Amplification),[5] single cell and bacterial culturing devices,[6–9] and a plethora of flow based sorting methods.[10–12] Continuous phase, pressure driven microfluidics is one of the most popular methods of actuating microfluidic devices.[13–16]

Multilayer PDMS microfluidic devices, since its introduction, have been instrumental in providing precise flow control of reagents.[17,18] Push up and push down valves use PDMS's inherent elasticity to create robust switches in a complex flow network.[19–21] Using these basic on-chip flow control components, complex devices have been built that are used for a slew of applications from a chemostat for culturing bacteria,[9] an on-chip MDA for haplotyping,[22] to a cell culture platform.[7] Even though such multilayer microfluidic chips, using push up or push down control elements, offer great power for precision measurement and analysis of biological samples and processes, they do have limitations. One such limitation is that the on-chip elastomeric valves can only act like digital switches, allowing or disallowing flow. The same valve cannot provide a range of analog actuation pressures to partially restrict a channel without requiring the user to manually adjust bulky, external pressure sources. When it is necessary to vary pressure and flow rates of multiple flows on the same chip, an on-chip method to create a range of pressures from a single, constant, external pressure source is preferred.

Other microfluidic based devices for converting digital concentrations to discrete levels of analog concentrations have been demonstrated.[23,24] They are all flow-based digital to analog converters (DACs) that use standard push up or push down digital shutoff valves. We present here the first microfluidic component that can provide DAC functionality at the pressure level. Our microfluidic DAC creates different pressures on-chip from a single, constant, external pressure supply. Just like an electronic DAC that converts digital voltage bits into corresponding analog voltages, this microfluidic serial DAC operates by converting digital pressure bits into

[a]*Departments of Bioengineering and Applied Physics, Stanford University and Howard Hughes Medical Institute, Stanford, California 94305, USA. E-mail: quake@stanford.edu; Tel: +1 (650) 721-2195*
[b]*Department of Electrical Engineering, Stanford University, Stanford, California 94305, USA*

† Electronic supplementary information (ESI) available. See DOI: 10.1039/c3lc41394b

analog pressures. Output pressures from such a microfluidic serial DAC can be used for applications where an independently addressable pressure array is required, or where variable pressures need to be maintained on chip. In addition, output pressures can be used to change flow channel cross sections and adjust flow resistances. Through on-chip tuning of flow rates, one can vary placement of laminar flow boundaries and generate arbitrary mixing proportions without having to design a new chip with altered geometries. As an example, controlling flow rates by tuning flow resistances prevents contamination caused by potential backflow. This property is an inherent advantage of controlling flow rates using the DAC compared to varying external pressure regulators.

Operational principles

At the most basic level, a microfluidic DAC generates an analog pressure to depress an elastic diaphragm. There are many possible electronic DAC architectures. Resistive DACs operate based on switching in or out resistor segments to generate desired current or voltage at the output. If each segment changes the output by one LSB (Least Significant Bit), the structure is called a thermometer DAC. If each segment produces output changes by increasing powers of 2, then the structure is called a binary-weighted DAC. Both of these DACs have a parallel structure with a predefined resolution set by the number of switchable segments. Serial DACs, on the other hand, do not have a predefined resolution. Their operation is based on capacitive ratios and charge transfer. Previous work has demonstrated creating analog pressures to deform a PDMS diaphragm using a binary-weighted structure for microlens applications.[25] Our microfluidic pressure DAC borrows its architecture from an electronic serial DAC because it has low complexity and a small number of required components (Fig. 1a). These two advantages translate into a small footprint and ease of fabrication.

The electronic serial DAC operates based on the principle of charge sharing, where actuation of a switch S3 connects C1

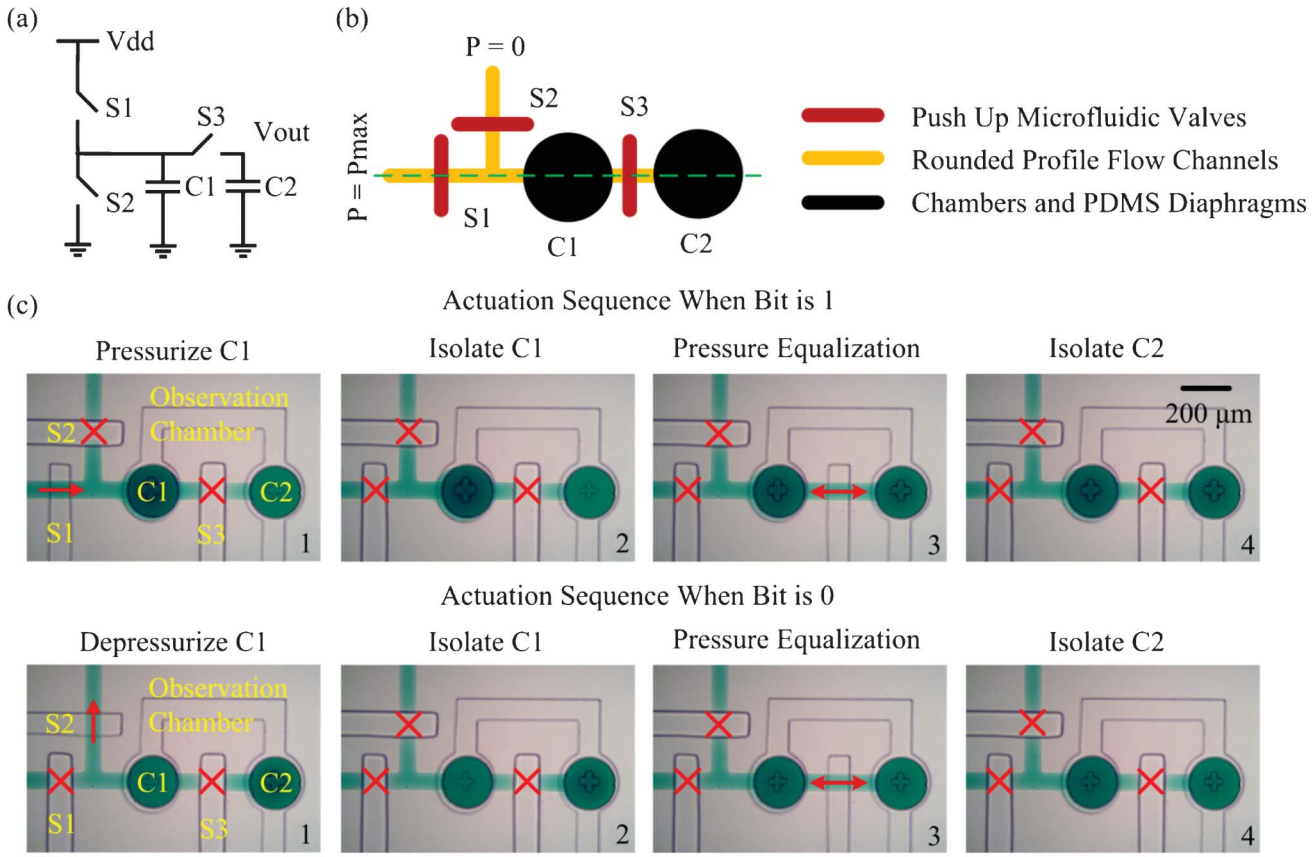

Fig. 1 Design and operating principle of the microfluidic serial DAC. (a) Circuit diagram of an electronic serial DAC. S1–S3 are switches often implemented with transistors. C1 and C2 are linear and matched capacitors. (b) Top view design of the microfluidic serial DAC including rounded fluidic channels (yellow) and cylindrical fluidic chambers (black) on the top layer and push up valves as switches (red) in the bottom layer. Pmax is connected to 10 psi. All pressures noted in our experiments are with respect to atmospheric pressure. (c) Actuation sequence for the microfluidic serial DAC. For each digit in a binary bit stream from LSB to MSB, a microfluidic serial DAC follows the 4 numbered steps shown. Flow channels are green while the control channels are transparent. High pressure comes from the left while atmospheric pressure comes from the top of each image. Red ''X'' means that the underlying flow channel is cut off. Observation chambers are used to provide space for membrane deformation.

and C2 and redistributes charge on both capacitors (Fig. 1a). Therefore the voltage on C2 during cycle $n + 1$ is the weighted average of the voltages on C1 and C2 during cycle n (eqn (1)).

$$V_{C2}(n+1) = \frac{C_1 V_{C1}(n) + C_2 V_{C2}(n)}{C_1 + C_2} \quad (1)$$

Assuming C1 = C2, the voltage on C2 after each charge sharing cycle is the average of the original voltages on the two capacitors (eqn (2)).

$$V_{C2}(n+1) = \frac{V_{C1}(n) + V_{C2}(n)}{2} \quad (2)$$

Furthermore, if the voltage on C1 is set to a digital 1 or 0 before actuating S3, the resulting voltage on C2 after charge sharing moves either half way closer to a digital 0 (if $V_{C1}(n) = 0$) or half way closer to a digital 1 (if $V_{C1}(n) = 1$) (eqn (3) and (4)).

$$V_{C2}(n+1) = \frac{V_{C2}(n)}{2} \qquad V_{C1}(n) = 0 \quad (3)$$

$$V_{C2}(n+1) = \frac{1 - V_{C2}(n)}{2} + V_{C2}(n) \qquad V_{C2}(n) = 1 \quad (4)$$

Using this principle, any voltage value on C2 between a digital 0 and 1 can be generated using a sufficient number of such charge sharing cycles. For the case where C1 equals C2, each charge sharing cycle (including first setting the voltage on C1 to a digital 1 or 0 followed by actuating S3 to equilibrate voltages on C1 and C2) can be represented by a binary bit in an arbitrarily long bit stream.

The proposed microfluidic serial DAC functions similarly. In the fluidic domain, pressure is analogous to voltage and molecules of water are analogous to charge. The concept of charge accumulation and sharing can be understood as accumulating and sharing volumes of water to achieve pressure equalization. Switches and capacitors in the electronic serial DAC are replaced by push up valves and capacitive chambers in the microfluidic serial DAC respectively (Fig. 1b). In terms of operation, fluidic valves S1 and S2 control whether C1 is pressurized to a high or low pressure. Then, opening and closing the fluidic valve S3 performs sharing of water molecules and pressure equalization (Fig. 1c). Similar to the electronic serial DAC, assuming that C1 = C2 and that both fluidic capacitors are linear, a sufficient number of pressure equalization cycles can be used to generate arbitrary pressures in C2 between 0 and the maximum applied pressure. Here, all pressures are measured with respect to atmospheric pressure. In order to generate an arbitrary pressure on C2, the pressure value is converted into binary code. Then the actuation sequence outlined in Fig. 1c is used for each bit in the bit stream from LSB to MSB (Most Significant Bit). Supplementary videos 1 and 2 demonstrate this operation for the four bit codes 0101 and 1110.†

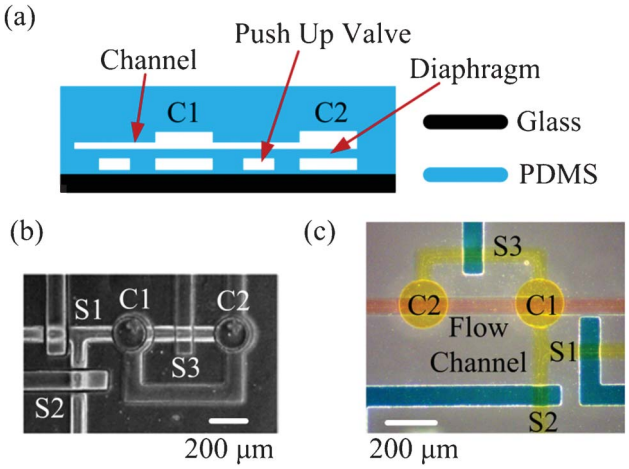

Fig. 2 Structure of the microfluidic serial DAC. (a) Cross section view of the microfluidic serial DAC cut along the dotted green line in Fig. 1b. (b) Top view of the fabricated device, showing capacitive PDMS membranes (C1 and C2) as well as push up valves acting as switches (S1, S2, and S3). (c) A microfluidic DAC containing the capacitive (yellow) layer and switch control (blue) layer located beneath a flow channel (red) to adjust flow resistance.

Material and methods

Fabrication uses standard multi-layer PDMS soft lithography process. The microfluidic serial DAC contains two layers. The top layer contains the capacitive chambers and channels that allow pressures to be transferred to the diaphragms. The bottom layer includes push up valves that are used as switches. SU8 and SPR (MicroChem) are first used to create molds on silicon. 25 μm high SU8 switches are patterned on the bottom layer. For the second layer, SPR is first used to create 10 μm rounded channels. In order to create the rounded channel profiles on the SPR mold, the corresponding wafer is baked overnight to facilitate reflowing of the SPR resist after lithography. Then 40 μm tall chambers are patterned using SU8. For PDMS chip fabrication, Sylgard or RTV PDMS (Dow Corning or RS Hughes) is used to mold both layers on the silicon master. A thick PDMS layer is created for the top layer and then bonded to a thin bottom layer spun onto the silicon mold. Thermal bonding at 80 °C joins the PDMS layers. Finally, the two layer structure is plasma bonded to a glass slide. Push-up valves are used in the DAC to increase the valves' ability to close flow channels so that lower switch line pressures can be used to actuate DAC switches. The cross section schematic and the top view of the fabricated device are shown (Fig. 2a and b).

In order to demonstrate the ability to control flow, a device was created where an additional flow layer with rounded channels is used as the top layer. Channels are placed over the DAC chambers so that DAC diaphragms act as pressure regulators by restricting the cross section of the top flow channels (Fig. 2c). This three layer PDMS microfluidic device still uses off-ratio thermal bonding between all layers except the interface between PDMS and glass, where plasma bonding is used. In this chip, the microfluidic serial DAC controls flow

rate through the deformation of flow channel cross sections, which effectively increases flow resistance.

Results and discussion

Testing of the microfluidic DAC is accomplished in two stages. Isolated devices are first assessed for their functionality and characteristics such as the transfer function, linearity, and frequency response. Then, multiple devices are integrated into simple flow channels to demonstrate the DAC's ability for flow control. During the first stage, a two layer PDMS device is fabricated that includes microfluidic serial DACs with different sized diaphragms. Incorporating devices with diaphragms of different diameters on the same chip can best remove device to device process variations and provide the most direct comparison of performance characteristics due to component differences.

Since the microfluidic serial DAC only functions with incompressible fluids, dead-end filling with water is performed on all devices. During actuation, each DAC is connected to external pressure sources *via* water-filled tubes (Tygon) and placed under a 40× inverted phase microscope (Leica DMI 6000B). Pneumatic valves (Pneumadyne) are used to deliver pressure bits to the device *via* custom software written in MATLAB (Mathworks). In this process, with a constant external pressure source of 10 psi, a 4-bit digital code is first passed to the microfluidic serial DAC using actuation sequence shown before (Fig. 1c). Upon completion of the sequence, the microscope objective is adjusted to acquire focus on the center of the C2 PDMS membrane. S1 and S3 are then opened so that the external pressure can be directly applied to C2's PDMS membrane. Then, external pressure is lowered until the same location on the diaphragm regains focus. Pressure applied through the external source, therefore, is assigned to the output pressure of the DAC with a 10 psi source and the particular input code.

Fig. 3 illustrates transfer function of the microfluidic serial DAC from 0 to 10 psi for 4 bit digital codes. The three curves represent devices with PDMS membranes whose diameters are 150 μm (green), 200 μm (red), and 250 μm (blue). All other device dimensions for the three microfluidic DACs are identical. From their transfer functions, the device with 250 μm capacitive diaphragm displays the smoothest output. As diameter of the PDMS membranes decrease to 200 μm and 150 μm, output of the device becomes less linear. In particular, transfer function of the 200 μm DAC shows a vertical kink when the MSB is switched from zero to one. For the 150 μm DAC, this vertical kink becomes more pronounced. In addition, there are smaller kinks when the second most significant bit changes from zero to one. These nonlinearities could likely be due to two possible causes: nonlinearity of the capacitors themselves and how well the two capacitors in each DAC are matched. We investigated the linearity of individual microfluidic capacitive membranes (ESI†) and found that for our range of component geometries and operation range,

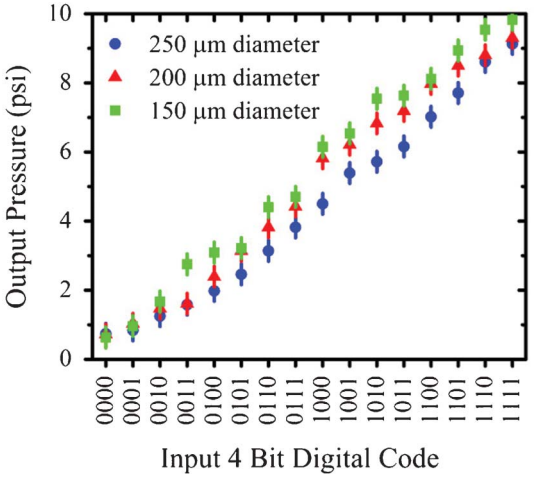

Fig. 3 Transfer function of the microfluidic serial DAC. The serial DAC architecture does not have an intrinsic limitation on resolution. We arbitrarily choose a 4 bit binary input code. The output is between 0 and 10 psi with respect to atmospheric pressure. The output pressure is determined by finding the pressure that, when directly applied to the PDMS diaphragm, creates the same deformation as a certain digital code. DAC with 250 μm membranes show most linear output whereas the DAC with 150 μm membranes display nonlinear behavior as well as vertical offset.

circular PDMS diaphragms act as linear capacitors (Supplementary Fig. 1).†

How well the two fluidic capacitors match is another important property that determines linearity of the output. In the microfluidic serial DAC, matching of the capacitors is achieved mostly through consistency of the micro-fabrication process and using the same geometry for both chambers. The dominant source of mismatch comes from different lengths and numbers of channels attached to the capacitive chambers. If C1 ≠ C2, the output pressure on C2 after each charge sharing cycle from eqn (2) would not be the average of original pressures on C1 and C2. Accumulation of this deviation would result in erroneous outputs. From Fig. 2b we notice that there are more channels connected to C1 than C2. This creates a larger C1 compared to C2 and causes vertical kinks to appear in the transfer functions when MSB is changed from 0 to 1. The significance of the mismatch depends on the size of parasitic fluidic capacitances compared to the linear PDMS membrane capacitance. To minimize the effect of asymmetric channel parasitic capacitances, we can match channel lengths attached to each capacitive diaphragm and carefully lay out the device to prevent fabrication related mismatches.

Another observation from Fig. 3 is that the transfer function of DACs with smaller diameters is larger than the transfer function of DACs with larger diameters for the same input code. Vertical offset in output pressures can be explained using the concept of volume injection. Similar to the idea of charge injected when an electronic transistor is switched off, a small volume of incompressible fluid is displaced when a valve is shut off (Fig. 4a). This injected volume creates some extra deformation of the PDMS mem-

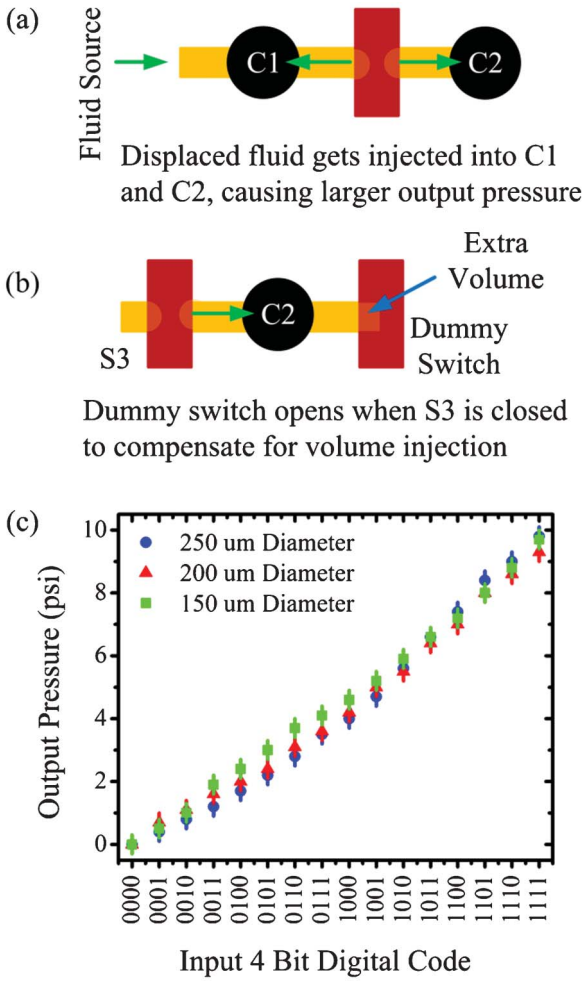

Fig. 4 (a) Fluid injection caused by extra volume pushed into the cylindrical chamber under C2 when push up valve (S3) closes can explain vertical offset in transfer functions. For a smaller membrane, injected fluid creates a larger Δz and thus a larger ΔP. (b) Fluid injection can be corrected with a dummy switch. Half of this dummy switch covers the flow channel (yellow) and assumes the opposite state of S3 in order to compensate for the extra volume (blue arrow) created or injected by the actuation of S3. (c) DAC transfer function for devices with matched capacitors and volume injection compensation. The output of the DAC is much more linear for all 3 capacitive membrane sizes. In addition, vertical offset due to volume injection is also mitigated.

brane, which translates into an increase in pressure. We can compensate for this injection using a dummy valve whose state is always opposite to the state of S3 (Fig. 4b). Just like top plate cancelation of charge injection in switch capacitor circuits, when S3 closes, the dummy valve would open, creating some room to store the extra fluid pushed into the capacitive chamber. The downside of this optimization would be a more stringent alignment requirement during fabrication.

Through modelling the two non-idealities mentioned above, we obtained C1 : C2 ratios for 150 μm, 200 μm, and 250 μm membranes as 1.19, 1.17, and 1.06. In terms of volume injection, we obtained resulting pressure offsets of 0.55, 0.12, and −0.52 psi (less than half of a LSB) for membrane diameters of 150 μm, 200 μm, and 250 μm respectively (ESI†). Both results are reasonable, which give us confidence in the underlying cause of transfer function nonlinearity. Following the non-ideality analysis, improvement was made to the previous design to create better matched capacitors even under small fabrication alignment errors. In addition, the new design incorporates a compensation method to adjust for volume injection. Transfer functions of the new DACs with different membrane diameters are quite linear for all devices tested (Fig. 4c). In addition, devices with different membrane diameters produce transfer functions that are very similar, validating the expectation that, to a certain degree, the operation of the microfluidic serial DAC should not depend critically on the capacitive membrane sizes.

Linearity of the microfluidic serial DAC describes its steady state characteristics. Its frequency response, on the other hand, determines how fast the device can operate and how fast the output pressures can change (Fig. 5). The serial DAC structure contains an intrinsic trade-off between resolution and speed. To maintain consistency, we test the frequency response with a 4 bit digital code 1010. As valve speeds increase, we monitor the entire valve actuation sequence time and the final output pressure. By convention, cutoff frequency is marked by the frequency at which the output pressure drops from its low frequency value by 3 dB. Frequency response plots for 200 μm and 250 μm DACs show cutoff frequencies of 1.1 and 3 Hz for a 4 bit input code, faster than all previously reported fluidic DACs.[23,24] Because the only difference between the DACs are sizes of the capacitive membranes, different cutoff frequencies imply that device operating speed is ultimately limited by time constant of the flow channel resistance and diaphragm capacitance instead of limited by the speed of switches S1, S2, and S3. Therefore, in order to increase device speed for a specific resolution, it is necessary to decrease either the resistance of flow channels connecting different capacitive chambers or decrease the capacitance of the PDMS membranes. Either of these optimizations would decrease linearity of fluidic capacitors. Thus, trade-off between linearity and actuation speed becomes an optimization space that one must choose for a specific application before fabrication. Another method to increase device operation speed is to reduce the total number of bits used, which reduces the number of valve actuation events needed. The trade-off here is decreased resolution, as the total number of analog levels is 2^B, where B is the number of bits used. Therefore, another optimization space exists between speed and resolution, though this can be decided post fabrication.

Since pressure provided by the microfluidic serial DAC is isolated in a pressurized PDMS chamber, in order for the DAC to be practical, the time that a device can maintain its pressure must be significantly longer than the time required to complete a refresh cycle. Fig. 5a shows that each refresh cycle can be completed in 1 s. Fig. 5b illustrates height decay of a pressurized PDMS membrane, which is an indirect measure of pressure decay inside the chamber. The criterion for decay time of a PDMS membrane is rather arbitrary. For a 4 bit

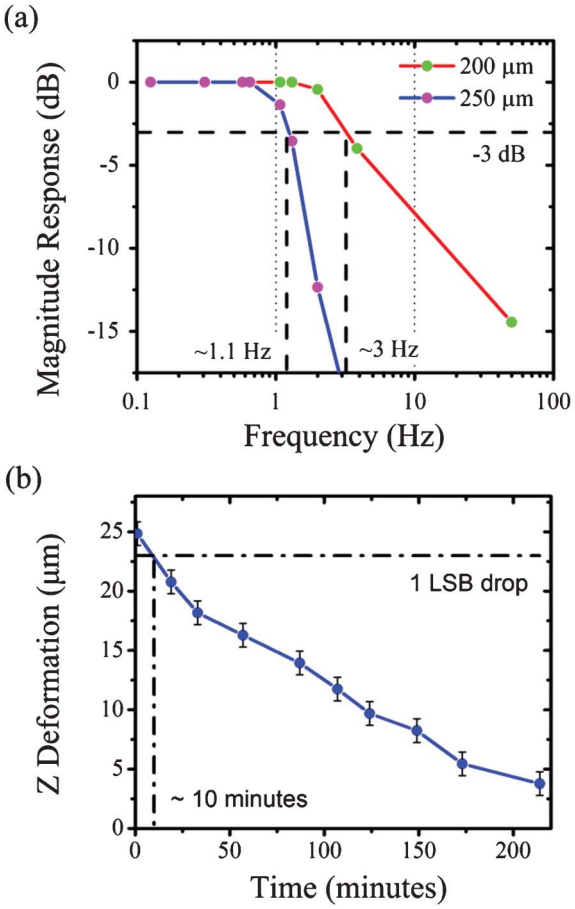

Fig. 5 (a) Frequency responses of two microfluidic serial DACs with diaphragm diameters of 200 μm (red line) and 250 μm (blue line). Both devices are fabricated on the same chip to minimize fabrication related differences such as membrane thickness and stiffness. All dimensions other than diaphragm diameters are identical. Instead of actuation time of the push up switches, different frequency responses for the two DACs reveal that the fundamental limiting factor is the time constant of the capacitive diaphragm and attached channels. (b) Decay of vertical deformation of a PDMS capacitive membrane over time is an indication of the ability of the DAC chambers to maintain a certain pressure. Pressure decay is mainly due to water evaporation since PDMS is permeable to gases. This test is performed at 25 °C and ~30% humidity. Graph shows that 1 LSB drop in pressure will require ~10 min. This time is more than 2 orders of magnitude longer than the time required to complete a 4 bit refresh cycle, which is less than 1 s.

application demonstrated in this work, we will designate 1 LSB drop to be the cutoff point of acceptable operational error. The pressure held on a DAC membrane can be maintained by ~10 min. Since this is more than 2 orders of magnitude longer than each refresh cycle, application of the DAC is not hampered by pressure decay over time. Alternatively, since pressure decay in PDMS chambers occurs due to evaporation, one can increase the hold time of a microfluidic DAC through the use of other fluids inside the capacitive chambers.

The microfluidic serial DAC can be applied to flow control applications where it is used to change flow resistances in order to establish the desired flow rate. Traditionally, geometry of a microfluidic device cannot be adjusted post fabricated. Thus, errors in channel dimensions can only be resolved by a new design cycle, costing time, money, and effort. The microfluidic DAC provides a method for post fabrication adjustment of flow resistances through tuning the vertical cross sections of flow channels. Using DAC tuning, small deviations or mismatches in different channels of a concentration gradient generator, for example, can be adjusted post fabrication to create desired output concentrations without resorting to another design and fabrication cycle. More importantly, microfluidic DACs can change flow resistances in real time, acting as a variable resistors in a fluidic network. Combined with image analysis tools, a closed loop, on-chip fluidic control system can be created. To illustrate this ability of the microfluidic serial DAC, we built a 'Y' junction with identical branches so that two different liquids, both actuated by 7 psi, join to form a laminar flow with a boundary in the middle of the channel. We then placed one DAC under each input branch to independently adjust the flow resistance of that branch (Fig. 6b). Using a 4 bit code and 10 psi input pressure, we can set laminar flow boundary to the desired location across the output channel (Fig. 6b and c).

There are many advantages to controlling flow using on-chip microfluidic DACs instead of adjusting off-chip pressure regulators. The first advantage is speed. Off-chip pressure regulators are often pneumatic and take on the order of seconds for output pressures to settle. In comparison, on-chip push up valves can be actuated in less than 100 milliseconds. Another advantage of using the microfluidic DAC has to do with control interface simplicity. With a small design overhead, microfluidic DACs can be easily integrated into any multilayer PDMS devices. Once fabricated, microfluidic DACs can be controlled using the same interface as normal push up valves. Only a simple valve actuation sequence is needed to adjust on-chip fluid flow. On the other hand, using off-chip methods to do real time flow rate adjustment often requires extra regulators and automation for manipulating those pressure regulators. The most important advantage for using on-chip DACs to control flow is stability and robustness. We demonstrate this advantage using a simple model that represents a 'Y' network, where resistances of the channels are abstracted into R_1, R_2, and R_3. Pressures at each point can be denoted as P_1, P_2, and P_x respectively (Fig. 6a). Output pressure by default is zero. Under laminar flow, we can assume that pressure drop, flow resistance, and flow rate form linear relationships. We show that P_x and flow rates through two input branches i_1 and i_2 can be written as in eqn (5)–(7) respectively. All parameters correspond to labelled components from Fig. 6a.

$$P_x = \frac{R_1R_2R_3}{R_1R_2 + R_1R_3 + R_2R_3}\left(\frac{P_1}{R_1} + \frac{P_2}{R_2}\right) \quad (5)$$

$$i_1 = \frac{R_2 + R_3}{R_1R_2 + R_1R_3 + R_2R_3}P_1 - \frac{R_3}{R_1R_2 + R_1R_3 + R_2R_3}P_2 \quad (6)$$

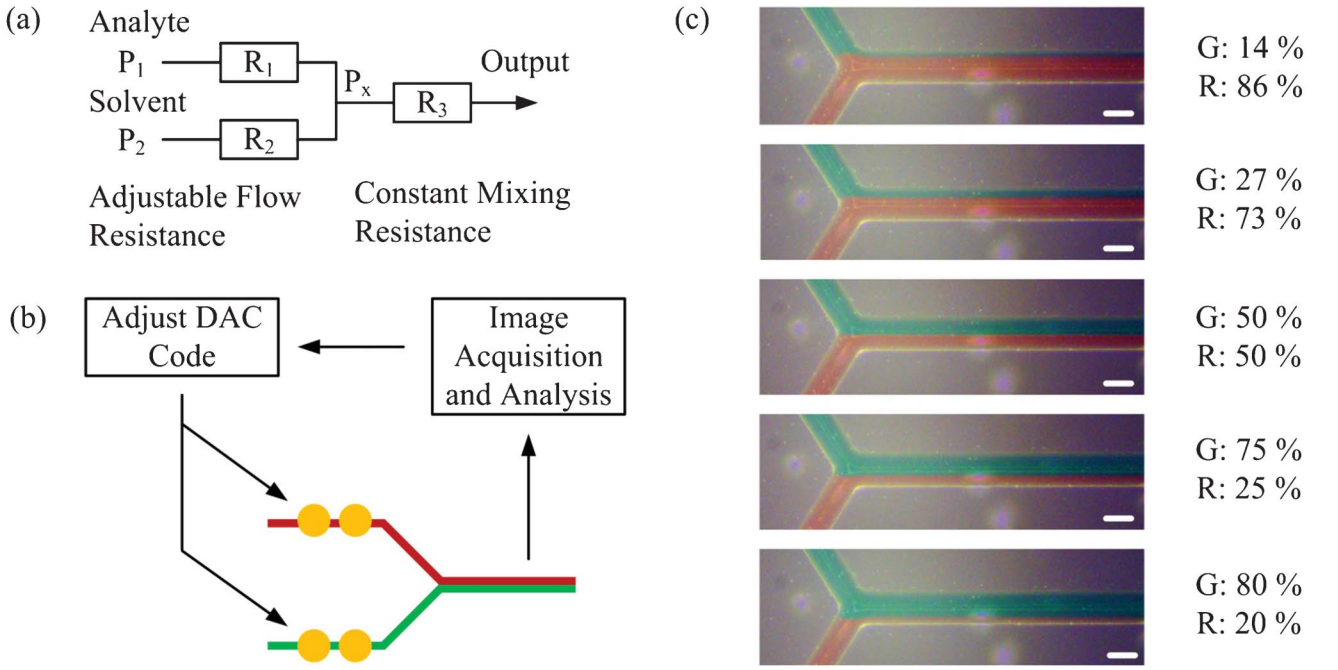

Fig. 6 Controlling flow resistances using microfluidic serial DAC. (a) Microfluidic serial DAC can be used to create variable fluidic resistors that are easily integrated into existing designs. Variable flow resistances allow tuning of output mixing using constant external flow pressures. (b) Coupled with a microscope and image processing capabilities, a feedback loop can be created that adjusts DACs' output pressures to obtain the desired flow profile. (c) Image sequence of different flow profiles created using two DACs at the input branches of a 'Y' junction. Boundary of the two laminar flows is placed at different locations across the flow channel through adjusting DACs' output pressures. White scale bars represent 100 μm.

$$i_2 = \frac{R_1 + R_3}{R_1R_2 + R_1R_3 + R_2R_3} P_2 - \frac{R_3}{R_1R_2 + R_1R_3 + R_2R_3} P_1 \quad (7)$$

Flow rate equations of the input branches show that if one blindly adjusts input pressures hoping to control output boundary between the two input laminar flows, it is possible that one of the two flow rates would become negative, resulting in backflow and contamination of reagents. In fact, for most microfluidic networks that involve joining of multiple inputs, R_3 is often much larger than R_1 and R_2. Therefore, even small pressure changes to P_1 or P_2 could lead to back flow in one of the branches. In our experiments, with $P_1 = P_2 = 6$ psi, we observe that small adjustment in P_1 or P_2 is enough to result in back flow in one of the input branches (Supplementary video 3†). Thus, output flow rates are sensitive to small pressures changes, which can lead to backflow and contamination. However, using on-chip microfluidic DACs to control flow rate effectively increases R_1 and R_2 depending on which DAC is used. Since R_1 and R_2 are only present in the denominator of eqn (6) and (7) respectively, increasing their values decrease i_1 and i_2 asymptotically to zero, but never negative (Supplementary video 4†). Therefore, using microfluidic DACs to control flow rate is a more stable and robust method, alleviating worries of backflow induced contamination.

Conclusions

We demonstrate the operation of a microfluidic serial digital to analog pressure converter that has the ability to create linear pressure outputs for controlling microfluidic flow resistances in multilayer PDMS devices. The microfluidic DAC allows on-chip, dynamic, and real time control without the need to adjust off-chip pressure regulators. At the same time, adjusting flow resistances using microfluidic DACs appear to be a more robust method than using off-chip pressure regulators. Combined with image analysis methods to complete the feedback loop, the microfluidic pressure DAC opens the door for accurate and analog control of flow rates in biological or chemical experiments. The process of integrating the microfluidic DAC into existing PDMS devices requires consideration for trade-offs between linearity, resolution, robustness, and speed. These characteristics are, in turn, controlled by diaphragm height, thickness, capacitive chamber height, channel cross section, and actuation pressure. The dynamic design space, simple architecture, and robustness make the microfluidic serial DAC a useful microfluidic component.

Acknowledgements

The authors of this work would like to acknowledge the help of Vladimir Kibardin for his help in simulating capacitance ratios

of the fluidic capacitors. The authors would also like to thank members of the Stanford Microfluidic Foundry for fabricating some of the designs used in this project.

References

1 E. A. Ottesen, J. W. Hong, S. R. Quake and J. R. Leadbetter, *Science*, 2006, **314**, 1464–1467.
2 H. C. Fan, Y. J. Blumenfeld, Y. Y. El-Sayed, J. Chueh and S. R. Quake, *Am. J. Obstet. Gynecol.*, 2009, **200**, 543.e541–543.e547.
3 L. Mazutis, A. F. Araghi, O. J. Miller, J.-C. Baret, L. Frenz, A. Janoshazi, V. R. Taly, B. J. Miller, J. B. Hutchison, D. Link, A. D. Griffiths and M. Ryckelynck, *Anal. Chem.*, 2009, **81**, 4813–4821.
4 F. Shen, W. Du, J. E. Kreutz, A. Fok and R. F. Ismagilov, *Lab Chip*, 2010, **10**, 2666–2672.
5 P. C. Blainey and S. R. Quake, *Nucleic Acids Res.*, 2011, **39**(4), e19, DOI: 10.1093/nar/gkq1074.
6 P. J. Hung, P. J. Lee, P. Sabounchi, R. Lin and L. P. Lee, *Biotechnol. Bioeng.*, 2005, **89**, 1–8.
7 R. Gomez-Sjoberg, A. A. Leyrat, D. M. Pirone, C. S. Chen and S. R. Quake, *Anal. Chem.*, 2007, **79**, 8557–8563.
8 P. Wang, L. Robert, J. Pelletier, W. L. Dang, F. Taddei, A. Wright and S. Jun, *Curr. Biol.*, 2010, **20**, 1099–1103.
9 F. K. Balagadde, L. You, C. L. Hansen, F. H. Arnold and S. R. Quake, *Science*, 2005, **309**, 137–140.
10 L. R. Huang, E. C. Cox, R. H. Austin and J. C. Sturm, *Science*, 2004, **304**, 987–990.
11 M. D. Vahey and J. Voldman, *Anal. Chem.*, 2008, **80**, 3135–3143.
12 M. M. Wang, E. Tu, D. E. Raymond, J. M. Yang, H. Zhang, N. Hagen, B. Dees, E. M. Mercer, A. H. Forster, I. Kariv, P. J. Marchand and W. F. Butler, *Nat. Biotechnol.*, 2005, **23**, 83–87.
13 K. Leung, H. Zahn, T. Leaver, K. M. Konwar, N. W. Hanson, A. P. Page, C. C. Lo, P. S. Chain, S. J. Hallam and C. L. Hansen, *Proc. Natl. Acad. Sci. U. S. A.*, 2012, **109**, 7665–7670.
14 M. Rhee and M. A. Burns, *Lab Chip*, 2009, **9**, 3131–3143.
15 L. M. Fidalgo and S. J. Maerkl, *Lab Chip*, 2011, **11**, 1612–1619.
16 J. A. Weaver, J. Melin, D. Stark, S. R. Quake and M. A. Horowitz, *Nat. Phys.*, 2010, **6**, 218–223.
17 C. L. Hansen, E. Skordalakes, J. M. Berger and S. R. Quake, *Proc. Natl. Acad. Sci. U. S. A.*, 2002, **99**, 16531–16536.
18 D. C. Leslie, C. J. Easley, E. Seker, J. M. Karlinsey, M. Utz, M. R. Begley and J. P. Landers, *Nat. Phys.*, 2009, **5**, 231–235.
19 I. E. Araci and S. R. Quake, *Lab Chip*, 2012, **12**, 2803–2806.
20 J. Melin and S. R. Quake, *Annu. Rev. Biophys. Biomol. Struct.*, 2007, **36**, 213–231.
21 T. Thorsen, S. J. Maerkl and S. R. Quake, *Science*, 2002, **298**, 580–584.
22 H. C. Fan, J. Wang, A. Potanina and S. R. Quake, *Nat. Biotechnol.*, 2011, **29**, 51–57.
23 F. Azizi and C. H. Mastrangelo, *Lab Chip*, 2008, **8**, 907–912.
24 L. Chen, F. Azizi and C. H. Mastrangelo, *Lab Chip*, 2007, **7**, 850–855.
25 P. Fei, Z. He, C. H. Zheng, T. Chen, Y. F. Men and Y. Y. Huang, *Lab Chip*, 2011, **11**, 2835–2841.

